UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,104	06/15/2005	Otto Steinbusch	US02 0610 US2	9255

24738 7590 04/02/2007	EXAMINER	
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION		
INTELLECTUAL PROPERTY & STANDARDS	MERANT, GUERRIER	
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SAN JOSE, CA 95131	ART UNIT	PAPER NUMBER
	2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)
Office Action Summary	10/539,104	STEINBUSCH, OTTO
	Examiner	Art Unit	
	Guerrier Merant	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/26/07*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

GUY LAMARRE
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)
1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's arguments/amendments with respect amended claims 1-7 & 12-15

and previously presented claims 8-11 filed 01/26/07 have been fully considered but they

are not persuasive. The Examiner would like to point out that this action is made final

(See MPEP 706.07a).

Response to Arguments

Applicant's submittal of 2/16/07 is not signed and thus is non-compliant.

In response to claim 1, Applicant contends that the prior art of record, **Cassetti et**

al., fails to teach *"setting and storage of bits in a test access port (TAP) controller"* and

"resetting a first bit to a known state in each of a plurality of TAP controllers."

In response to claim 12, Applicant contends that **Cassetti et al.** fails to teach the

limitation *"each of the plurality of TAP controllers having at least one switch bit and the*

routing logic selectively connecting to one of the plurality of TAP controllers based at

least in part on the state of the switch bits."

The Examiner respectfully disagrees. **Cassetti et al.** clearly teaches the limitation of

"setting and storage of bits in a test access port (TAP) controller" *(col. 5, lines 61-67),*

and the limitation of *"resetting a first bit to a known state in each of a plurality of TAP*

controllers." (col. 6, lines 1-10). Moreover, **Cassetti et al.** teaches *"each of the plurality*

of TAP controllers having at least one switch bit (item 22 & 36- fig. 1&2) and the routing

logic (CHIP LEVEL TAP LINK MODULE, item 40, fig. 1& 2- col. 4, lines 53-67 & col. 5,

lines 1-6) selectively connecting to one of the plurality of TAP controllers based at least

in part on the state of the switch bits." The Examiner notes that the <u>*switch bit*</u> that the

Applicant is claiming is the same "one bit register" claimed in claim 1.

Thus, the Examiner maintains rejections with respect to amended claims 1-7 &

12-15 and previously presented claims 8-11. **<u>Cassetti et al.</u>** teaches all the limitations

that the Applicant suggests distinguish from prior art.   Therefore, it is the Examiner's

conclusion that amended claims 1-7 & 12-15 and previously presented claims 8-11 are

not patentably distinct or non-obvious over the prior art of record as presented.

The Examiner notes that previous Office Action was mistakably cited due to

typographical error but that does not necessitate new ground of rejection *(See MPEP*

1207.03).

There is no new ground of rejection when the basic thrust of the rejection remains the same such that an

appellant has been given a fair opportunity to react to the rejection.

See In re Kronig, 539 F.2d 1300, 1302-03, 190 USPQ 425, 426-27 (CCPA 1976). Where the statutory basis

for the rejection remains the same, and the evidence relied upon in support of the rejection remains the same, a

change in the discussion of, or rationale in support of, the rejection does not necessarily constitute a new

ground of rejection. Id. At 1303, 190 USPQ at 427 (reliance upon fewer references in affirming a rejection

under 35 U.S.C. 103 does not constitute a new ground of rejection).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form

the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public

use or on sale in this country, more than one year prior to the date of application for patent in the United

States.

Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by **Casseti et al.**

(US 6,311,302 B1).

Claim 1: **Casseti et al. (US 6,311,302 B1)** discloses a method of coupling a plurality of

test access port (TAP) controllers to a single external interface *(col. 3, lines 6-19, see*

fig. 1), comprising: resetting a first bit in each of plurality of TAP controllers *(col.6, lines*

1-10) a known state *(on/off or 0 or 1)*; producing a first signal based, at least in part, on

the state of the first bit in each of the plurality of TAP controllers *(depending upon the*

command loaded into the internal TLM register, the TLM module enables or disables

various TAPs in a system by controlling TMS- col. 2, lines 21-50); selecting one of the

plurality of TAP controllers based, at least in part, on the first signal *(this functionality is*

done by the Chip-level TML 40- see figs.1 or 2); coupling an external input terminal to

an input terminal of the selected one of the plurality of TAP controllers; and coupling an

output terminal of the selected one of the plurality of TAP controllers to an external

output terminal *(col.4, lines 53-65)*.

Claim 2: The method of claim 1, wherein the TAP controller comprises a finite state

machine and a plurality of registers *(col. 5, lines 7-28)*.

Claims 3 and 4: **Casseti et al.** discloses a method as in claim 2 above, further

comprising toggling *(inverting)* the first bit in the selected one of the plurality of TAP

controllers; and repeating steps (b) through (e) *(col. 5, lines 56-67 & col. 6, lines 1-10)*.

Claims 5 and 6: **Casseti et al.** discloses a method as in claim 3 above, wherein the

plurality of TAP controllers are disposed on a single integrated circuit and the first signal

is produced within the single integrated circuit *(see figs. 1 & 2 for connection- col. 4,*

lines 53-68 & col. 5, lines 1-6).

Claim 7: **Casseti et al.** discloses a method as in claim 6 above, further comprising

receiving from a source external to the single integrated circuit, a clock signal *(see figs*

1& 2 wherein externals signals TCK, TMS, TDI, TRST are being received by the

integrated circuit 10).

Claims 8-10, 12 and 13: **Casseti et al.** discloses an integrated circuit *(item 10, Figs. 1 &*

2), comprising: a plurality of functional blocks *(items 12 & 14, Figs. 1 & 2)*, each

functional block having a test access port (TAP) controller coupled thereto *(items 16,*

18, 30, 32- Figs. 1 & 2); each TAP controller including a first register bit *(items 20,22 &*

36,34- Figs. 1 & 2), each first register bit adapted to produce a known output state in

response to a reset signal *(depending upon the command loaded into the internal TLM*

register which is resetting after each instruction, *the TLM module enables or disables*

various TAPs in a system by controlling TMS- col. 2, lines21-50 & col. 6, lines 1-10),

each first register bit further adapted to toggle in response to a register write operation; and routing logic (CTLM, item 40; fig. 1&2) adapted to selectively provide, based at least in part on the state of the plurality of first register bits, a communication path between an external input signal source and an input terminal of a selected one of the TAP controllers (col. 5, lines 56-67 & col. 6, lines 1-10, see Figs. 1&2).

Claim 11: **Casseti et al.** discloses an integrated circuit as in claim 9 above, wherein a transition between the selectively provided communication paths is transparent to an external observer (col. 4, lines 53-66- once an instruction is loaded, the TLM 40 selects which Tap to access without the help of user or observer).

Claim 14: **Casseti et al.** discloses an integrated circuit as in claim 13 above, wherein the each of the plurality of TAP controllers has a second input terminal adapted to receive a clock signal (TCK, fig. 1), a third input terminal adapted to receive mode select signal (TMS, fig.1), and a fourth input terminal adapted to receive a reset signal (TRST, fig.1); wherein the plurality of second input terminals are coupled in common, the plurality of third input terminals are coupled in common, and the plurality of fourth input terminals are coupled in common (col. 5, lines 7-28).

Claim 15: **Casseti et al.** discloses an integrated circuit of claim 14 above, further comprising a chain bit (item 22 figs. 1& 2) disposed in a first one of the plurality of TAP controllers.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10: 30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Guy Lamarre can be reached on (571) 272-3826. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

/Guerrier Merant
03/13/07